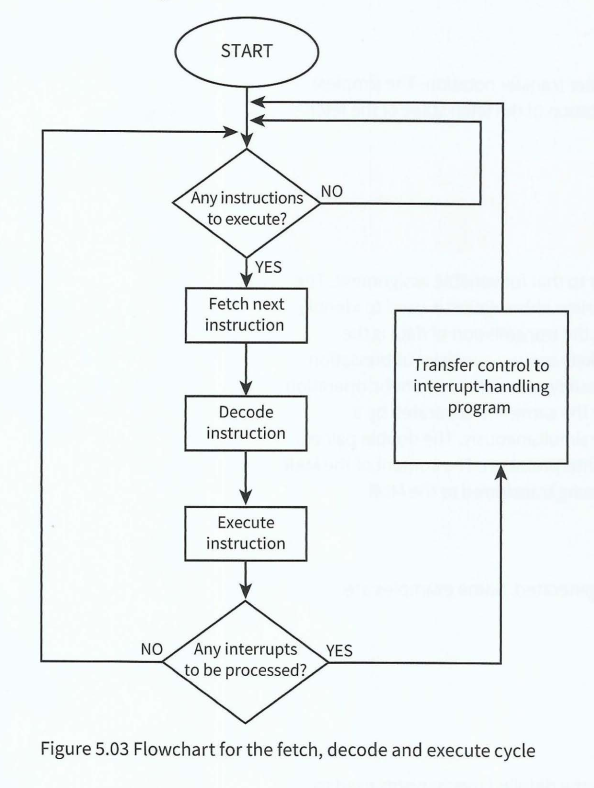
* Ch.5
* 5.01 The Von Neumann model of a computer system
* There is a processor, a central processing unit.
* The processor has direct access to a memory.
* The memory contains a 'stored program' (which can be replaced by another at any time) and the data required by the program.
* The stored program consists of individua l instructions.
* The processor executes instructions sequentially.
* 5. 02 Central processing unit (CPU) architecture
* Components of the CPU
* Arithmetic Logic Unit（ALU）
* Responsible for any arithmetic or logic processing that might be needed when a program is running
* Register
* Because its proximity to the ALU, it allows very short access times
* Limited storage capacity typically (16, 32 or 64 bits)
* Accumulator (general-purpose of registers)
* A general-purpose register that stores a value before and after the execution of an instruction by the ALU
* Current instruction registers (CIR)
* Stores the current instruction while it is being decoded and executed
* Index registers (IX)
* Stores a value; only used for indexed addressing
* Memory address registers (MAR)
* Stores the address of a memory location which is about to have a value read from or written to
* Memory data (buffer) register (MDR/MBR)
* Stores data that has just been read from memory or is just about to be read from
* Program counter (PC)
* Stores the address of where the next instruction is to be read from
* Status registers (SR)
* Contains individual bits that are either set or cleared
* 5. 03 The system bus
* The address bus
* A component that carries an address to the memory controller to identify a location in memory which is to be read from or written to
* The data bus
* A component that carries data to and from processor
* Word
* A small number of bytes handled as a unit by the computer system
* The control bus
* The universal serial bus (USB)
* A hierarchy of connections is supported
* The computer is at the root of this hierarchy and can handle 127 attached devices
* Devices can be attached while the computer is switched on and are automatically configured for use
* The standard has evolved, with USB 3.0 being latest version

Register transfer notation is used to describe data transfers.

e.g.

3 examples

Square brackets stand for the content of the register is being moved possibly with some \_arithmetic operation\_ being applied.

Semi-colon stands for the two transfers take place simultaneously.

Double pair of brackets stand for needing careful interpretation.

Fetch-execute cycle

Full name: fetch, decode and execute cycle.

(And the copy of the graph here)

Fetch stage: 3steps

**1** This address in the program counter is transferred within the CPU to the MAR.  
**2** During the next clock cycle two things happen simultaneously:  
the instruction held in the address pointed to by the MAR is fetched into the MDR  
• the address stored in the program counter is incremented.  
**3** The instruction stored in the MDR is transferred within the CPU to the CI R

Decode stage:3steps

The instruction stored in the CIR is received as input by the circuitry within the control unit.

Control unit will send signals to the appropriate components according to the type of instruction.

ALU will be activated if the instruction requires arithmetic or logic processing.

Execute stage:CHAPTER6